ANALYTIC DESIGN OF HIGH EFFICIENCY HARMONIC LOADING OSCILLATOR USING HARMONIC TWO SIGNAL METHOD

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ABSTRACT

A 61% *DC-to-RF* conversion efficiency oscillator with very low bias of 2.0 V is designed in 1.86 GHz. To obtain maximum DC-to-RF conversion efficiency, DC operating point is chosen in class AB with the second harmonic loading. The maximum efficiency and output power are analyzed and predicted very fast through a novel HTSM(Harmonic Two Signal Method) under class AB or B bias condition. Harmonic components effects on the oscillators, self-oscillating condition, and DC current change as the RF drive level are also analyzed through HTSM.

1. INTRODUCTION

The design method of the output power or DC-to-RF conversion efficiency of microwave oscillators is drawing considerable interests in some applications such as active antennas [1] and space power combiners [2]. Generally, solid-state microwave transistors provide the more efficiency than microwave diodes. Typical MESFET oscillator efficiency is of the order of 20% and HEMT oscillator has somewhat higher efficiency than MESFET oscillator. In order to design a high efficiency oscillator, it is required to select the optimum DC bias condition and RF drive level. In view of DC bias point, class AB or class B is preferred rather than class A due to its less DC current consumption. However class AB or class B bias has some problems in application to the oscillator. The first, the loop gain of which may have less than one because the transconductance gain is very small at this bias point. And that may give rise to the result that the start-up condition is not be achieved. And the second, near pinch-off point, operating RF signal contains strong harmonic components, which become the cause of discrepancy between the quasi-linear(or large-signal *S*-parameters) design and the experiment.

A oscillator design method was introduced by Kotzebue [4], in which the optimized oscillator design was determined by the information based on experimentally optimized amplifier. However his study did not take into account the effects of harmonic terminations. In class AB or B oscillator, the second harmonic load significantly influence the output power[3]. So, the second harmonic loading is of great interest in the high-efficiency oscillator.

This paper presents an analytical design method of high efficiency oscillator. HTSM is presented to predict the DC-RF efficiency, the output power, and DC bias shift in steady state of oscillator with the active device used as the power amplifier. The output load impedance is determined by the harmonic load line of the class F amplifier, which maximize the drain efficiency of power amplifier with harmonic terminations. In order to verify the presented method, high efficiency HEMT oscillator with low bias of 2V has been implemented and tested.

2. MAXIMUM EFFICIENCY ANALYSIS WITH HARMONIC TWO SIGNAL METHOD

2.1. Harmonic Two Signal Method

It is difficult to optimize the microwave transistor oscillator because there are many possible configurations and the tunning of the embedding circuit elements changes the oscillation condition. However a microwave power amplifier is more easier to optimize than the oscillator. In power amplifier, only two variables are required to be optimized; the output load impedance, and RF drive level. And there are many theories in determining the output load such as (harmonic) load-pull, tuned load-line, harmonic load line and, and so on. The concept of HTSM is that a transistor used as an amplifier under the optimized RF voltages and cur-

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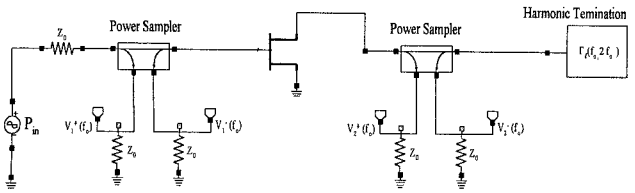

Figure 1: HTSM(Harmonic Two Signal Method) schematic for analysis the highest efficiency oscillator

rents to maximize the outward net-power, delivers the maximum output power as an oscillator if the operation conditions of the active transistors between the amplifier and the oscillator are same. In Fig. 1, $V_i^+(nf_o)$ and $V_i^-(nf_o)$ are the n-th harmonic incident and reflected waves at input($i = 1$) and output($i = 2$) ports. Where $V_2^+(f_o)/V_2^-(f_o)$ and $V_2^-(2f_o)/V_2^+(2f_o)$ represent the fundamental and the second harmonic reflection coefficient respectively. In HTSM, the total power that active device produces is

$$P = \{|V_1^-(f_o)|^2 - |V_1^+(f_o)|^2\} + \{|V_2^-(f_o)|^2 - |V_2^+(f_o)|^2\}/Z_o, \quad (1)$$

where Z_o is the characteristic impedance of measurement system. The active device in oscillation behavior will deliver the power of Eq.(1) to the load, if operation conditions of the two active transistors in oscillator and amplifier have the same operation.

2.2. Optimum Harmonic Load Line for High Efficiency Oscillator with low Drain Bias

The optimum load impedance for maximum drain efficiency is broadly studied at given bias in power amplifiers. Improvement of DC-RF efficiency is generally obtained by using class AB or B amplification. In such class, the pulsed drain current waveform generated while the drain voltage is maintained sinusoid. This means that harmonic voltages are shorted. Furthermore as the drain voltage goes to a square-wave, the improvement of the output power and efficiency is obtained in particular low drain bias[5]. In this paper, considering the implementation of the load impedance, the fundamental and the second harmonic impedance are taken into account. The optimum load is given as follows.

$$R_{opt}(f_o) = \frac{8}{\pi}\frac{V_{ds} - V_{sat}}{I_{max}}, \ and \ R_{opt}(2f_o) = 0 \quad (2)$$

Fig.2 shows the equivalent circuit for the HEMT with parasitic elements. In Eq.(2), R_{opt} is the impedance looking into the load at the drain current source. In order to compensate the parasitic elements and to apply

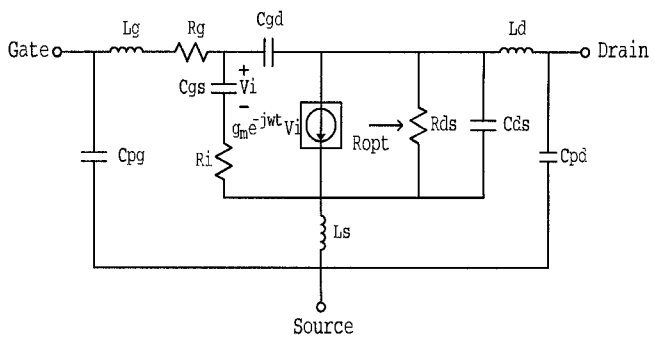

Figure 2: The position of the fundamental and harmonic load impedance

harmonic loading theory at the terminal, the terminal impedance for the R_{opt} should be de-embedded. The terminal admittance compensating for the parasitic elements is as follows

$$Y_L(nf_o) = \frac{1}{\frac{1}{\frac{1}{R_{opt}} - jn\omega C_d} - jn\omega(L_d + L_s)} - jn\omega C_{pd}. \quad (3)$$

where, n is the order of harmonics. Fig.3 shows the results of HTSM with the harmonic load of (3). 3. From Fig.3, we note that class B oscillator has significant increase of DC drain current as the input incident power is increase. In proportion to the DC drain current, the output power and the efficiency are increase until the gate-source Schottky barrier is turned on. The maximum DC to RF efficiency rises at the very point of Schottky barrier is turned on, while maximum output power is observed at slightly upper the turn-on point. From the Fig.3, the RF drive level of the highest efficiency oscillator is determined as the incident power that make the gate-source barrier turn-on.

2.3. Net-Power Gain of Two Port Device

Since the small signal gain of active device with bias at class AB or B is very small, the start-up condition of oscillator should be investigated in class AB or B oscillator. Since an oscillation is triggered by small signal noise meeting the positive feedback condition, and grows up until it reaches the steady-state condition. The net-power gain of device in oscillator can be defined as follows

$$G_{net} = \frac{|V_1^-|^2 + |V_2^-|^2}{|V_1^+|^2 + |V_2^+|^2}. \quad (4)$$

This gain means the ratio of the outward power to the inward power of device. Usually the oscillators are de-

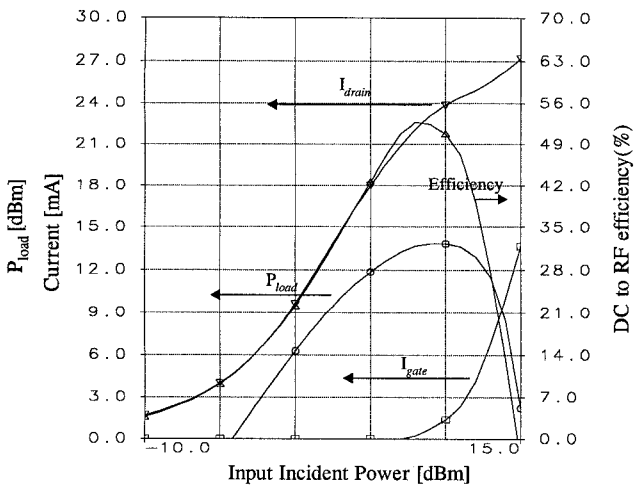

Figure 3: Analysis result of HTSM(Harmonic Two Signal Method) at ($V_{gs} = -0.5V$, $V_{ds} = 2V$)

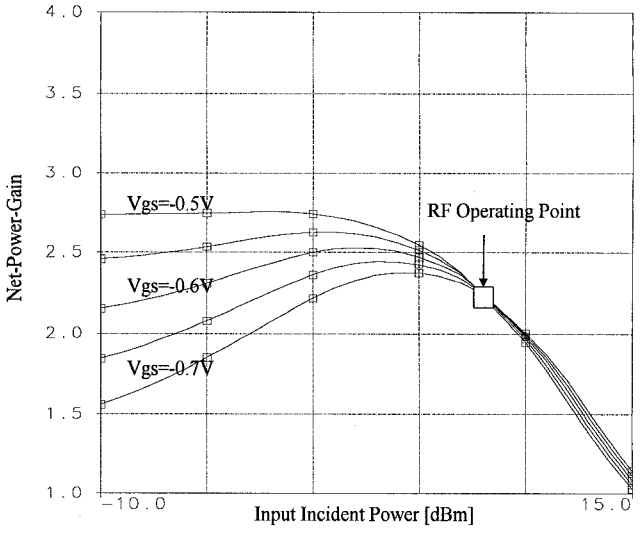

Figure 4: Net-power gain versus input incident power at various gate voltage bias

signed using the one-port negative impedance method, in which the loop gain is described as the reflection coefficient. However transistor is a real two-port device. Therefore, to look upon the transistor with feedback elements as an one-port negative impedance, the signal growing-up process in transistors should be known. The net-power gain defined as Eq.(4) contains the two-port information of the incident and reflected power at the gate-source and the drain-source. Since a transistor is basically the voltage(current)-controlled current source with parasitic elements, the power relationship at input and output is important to the design of oscillator. At the steady-state condition, the loss of embedding networks should be the same as that of the net-outward power of active transistor. Therefore, in order to reach the steady-state oscillation condition, the net-power gain at the start-up must be larger than net-power gain at operating incident power level in HTSM. In Fig.4, if RF operation point is determined at the point marked as blank box, oscillators biased with $V_{gs} = -0.5V$ and $V_{gs} = -0.6V$ can reach the steady-state oscillation condition, but oscillators with bias at which V_{gs} is smaller than $-0.6V$ cannot reach to the designed steady-state. Net-power gain G_{net} depends on the gate voltage in oscillator biased at near pinch-off voltage.

2.4. External Embedding Circuit Synthesis

With the predetermined input incident-wave power and harmonic load line in the HTSM, it is possible to obtain the values of all elements of the generalized six basic oscillator configurations; three shunt topologies and three series topologies. The fundamental terminal voltages at input and output are

$$\begin{aligned} V_i(f_o) &= V_i(f_o)^+ + V_i(f_o)^- \\ I_i(f_o) &= \{V_i(f_o)^+ - V_i(f_o)^-\}/Z_o \end{aligned} \quad (5)$$

where, i=1,2, and Z_o is the characteristic impedance of measurement system. Since output harmonic loads are reactively terminated in HTSM and ideal power sampling on simulation is used, the characteristic impedance of measurement system does not effect the terminal voltages and currents.

3. OSCILLATOR DESIGN AND PERFORMANCE

This design procedure was demonstrated using a Fujitsu HEMT, FHX35LG, at 1.86 GHz. Table 1 illustrates the specifications of HEMT used in this paper. To realize the harmonic load in embedding networks, the source impedance is shorted at $2f_o$, and $\Gamma_l(2f_o)$ is synthesized in only drain impedance. And the effects of the second harmonic impedance of gate reactance, $X_g(2f_o)$, is neglected. The impedance and the reactance are connected to the transistor are shown in Fig5.

The efficiency of 61% was obtained by pulling the gate voltage to -1.5 V, which was the maximum efficiency over all operating points. The maximum output power of 14.46 dBm obtained at $V_{gs} = -0.5V$. Since 1 dB saturated output power of this device is about 14 dBm, the maximum output power was occurred when gate-source Schottky barrier was turn on slightly($I_g = 2.9\ mA$) . Self-oscillation mode was observed when the gate bias voltages higher than -0.65 V. Fig.6 plots efficiency and output power as a function of gate bias. Experimental

Table 1: The specification of HEMT used in design

Iterms	FHX35LG
Gate Length, L_g	0.25 um
Gate Width, W_d	280 um
1-dB Saturation Power P_{1dB}	14 dBm
Gain-Bandwidth freq.f_t	35 GHz
Maximum Drain CurrentI_{max}	55.4 mA
Gate Turn-on voltage V_ϕ	0.6 V
Saturation Drain voltageV_{sat}	0.54 V
Pinch-off Gate voltageV_p	-0.55 V

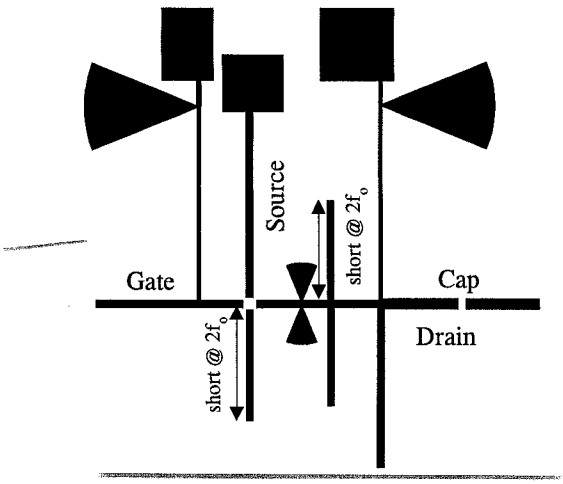

Figure 5: Circuit schematic of the high efficiency oscillator with low drain bias.

data agree well with the result of prediction through HTSM analysis. Table 2 and 3 show the comparison between the measurement and the prediction by the proposed HTSM. Good agreement between the HTSM prediction and measurement data is obtained

4. CONCLUSIONS

A systematic design method has been presented for high efficiency oscillator. The maximum efficiency and maximum output power for a given active device can be predicted through the HTSM. For the optimum RF drive level, embedding networks could be derived by fundamental frequency components of currents and voltages at input and output ports, which include the nonlinearity, DC bias-shift, and harmonic loading effects. This procedure is analytic so that it is very fast. A HEMT oscillator was demonstrated to verify the design approach. At 1.86 GHz, an output power of 14.46 dBm and maximum efficiency of 61% was obtained. This is the record data for the low drain bias of 2.0 V in L-band.

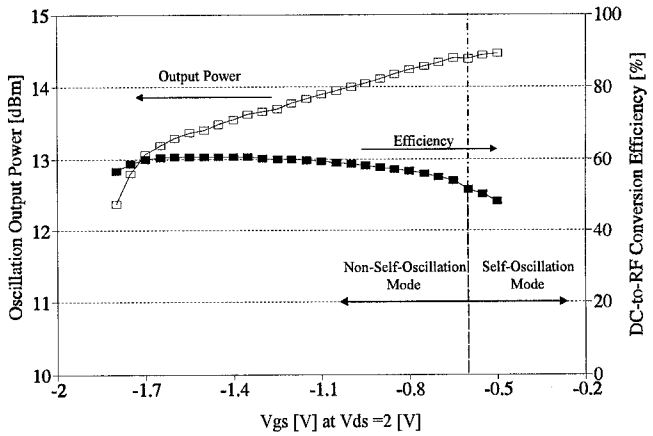

Figure 6: Experimental results

Table 2: Comparison between HTSM and measured data at $V_{gs} = -0.5V$

$V_{gs} = -0.5V$	HTSM Analysis	Measured
output power	13.62 dBm	14.46 dBm
DC/RF Efficiency	51.50 %	48.32 %

Table 3: Comparison between HTSM and measured data at $V_{gs} = -0.65V$

$V_{gs} = -0.65V$	HTSM Analysis	Measured
output power	13.58 dBm	14.40 dBm
DC/RF Efficiency	52.70 %	53.84 %

5. REFERENCES

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